REMARKS

Claims 1-22 were pending in this application.

Claims 1-22 have been rejected.

Claim 14 has been amended.

Claims 1-22 remain pending in this application.

Reconsideration and full allowance of Claims 1-22 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to Greenley et al. ("*Greenley*") in view of U.S. Patent No. 5,619,668 to Zaidi ("*Zaidi*"). The Applicant respectfully traverses this rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability,

then without more the Applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. (*MPEP § 2142*).

Claims 1 and 14 recite a "load store unit" capable of transferring a first data value from a "data cache" to a "target one of [a] plurality of registers" during execution of a load operation. Claims 1 and 14 also recite a "shifter circuit" capable of shifting, sign extending, or zero extending the first data value "prior to loading [the] first data value into [the] target register." In addition, Claims 1 and 14 recite "bypass circuitry" capable of "transferring [the] first data value from [the] data cache directly to [the] target register without processing [the] first data value in [the] shifter circuit."

Claims 1 and 14 are crystal clear – the "shifter circuit" can process a data value before

the data value is loaded from a data cache into a target register. Also, the "bypass circuitry" can transfer the data value from the data cache directly to the target register without the data value being processed by the "shifter circuit" (thereby bypassing the shifter circuit).

Both *Greenley* and *Zaidi* fail to disclose, teach, or suggest a structure that allows a data value to be transferred either (i) from a data cache to a target register through a shifter circuit, or (ii) directly from the data cache to the target register while bypassing the shifter circuit.

In *Greenley*, all data passes from the data cache 180 through the aligning unit 170 and the sign extension unit 160 into the register files 150. Similarly, in *Zaidi*, the Office Action asserts that shifting is performed in various multiplexors (such as multiplexors 18-19), and all data from the register file 13 passes through the multiplexors 18-19.

Because of this, both *Greenley* and *Zaidi* recite that all data passes through a shifter. *Greenley* recites that all data passes through a shifter (the alignment unit 170 and/or the sign extension unit 160) before the data is stored in a register file, while *Zaidi* recites that all data passes through a shifter (the multiplexors 18-19) after the data is stored in a register file. Neither reference discloses, teaches, or suggests a structure where a data value can either be (i) transferred from a data cache to a target register through a shifter circuit, or (ii) directly transferred from the data cache to the target register (while bypassing the shifter circuit).

At most, *Zaidi* might motivate a person skilled in the art to (i) move the aligning unit 170 and/or sign extension unit 160 of *Greenley* to lie between the register files 150 and the processor 100 of *Greenley*, or (ii) omit the aligning unit 170 and/or sign extension unit 160 of *Greenley* and insert the multiplexors 18-19 of *Zaidi* between the register files 150 and the processor 100 of

Greenley. Either modification would allow all data to pass through a shifter (the aligning unit 170 and/or sign extension unit 160 of *Greenley* or the multiplexors 18-19 of *Zaidi*). *Zaidi* only allegedly discloses placing a shifter after a register file, where all data passes through the shifter. As a result, *Greenley* could only be modified using *Zaidi* so that all data from the register files 150 passes through a shifter. Either modification would fail to disclose, teach, or suggest a structure where a data value can either be (i) transferred from a data cache to a target register through a shifter circuit, or (ii) directly transferred from the data cache to the target register (while bypassing the shifter circuit).

In addition, the Office Action argues that the proposed motivation to combine *Greenley* and *Zaidi* is that the proposed modification to *Greenley* helps to reduce pipeline stalls by "eliminating the time required to both read data and align the data from the resisters." (*Office Action, Page 14, Section 34*). However, the structure of *Zaidi* would not eliminate the time required to both "read data" and "align the data." *Zaidi* is directed to a system for bypassing a register file, not for bypassing any type of "alignment" circuit. In fact, the Office Action asserts that multiplexors 18-19 perform shifting operations, and the system of *Zaidi* is designed to always provide data to the multiplexors 18-19 (whether or not the data bypasses the register file 13). *Zaidi* in no way discloses, teaches, or suggests that the multiplexors 18-19 (which allegedly perform "alignment" operations) may be bypassed. The Patent Office cannot rely on the alleged elimination of an "alignment" operation in *Zaidi* as motivation to modify *Greenley* with *Zaidi* because *Zaidi* never discloses, teaches, or suggests bypassing an alignment operation.

As a result, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest

"bypass circuitry" capable of "transferring [a] first data value from [a] data cache directly to [a] target register without processing [the] first data value in [a] shifter circuit" as recited in Claims 1 and 14. Therefore, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest the Applicant's invention as recited in Claims 1 and 14.

Claim 10 recites transferring a first data value either (i) "from [a] data cache to a shifter circuit," where the shifter circuit shifts "the first data value prior to loading the first data value into [a] target register," or (ii) "from the data cache directly to the target register without processing the first data value in the shifter circuit." As shown above, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest these elements of Claim 10. As a result, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest the Applicant's invention as recited in Claim 10.

For these reasons, the Office Action has not established a *prima facie* case of obviousness against Claims 1, 10, and 14 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 1-22.

II. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Aug. 30, 2005

William A. Munck
Registration No. 39,308

P.O. Box 802432
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *wmunck@davismunck.com*